CONFIDENTIAL

OV5116 Series

SINGLE IC CMOS MONOCHROME CAMERA WITH ANALOG OUTPUT

Features

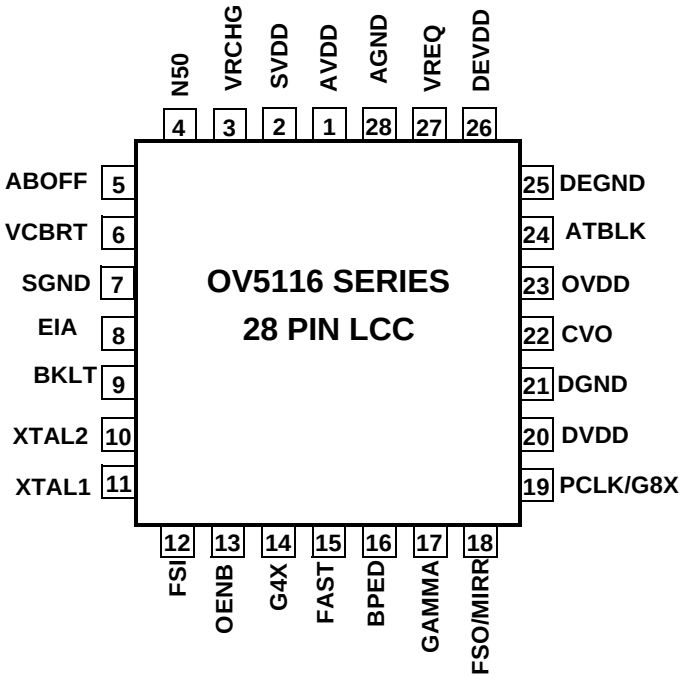
- **Single chip 1/4 inch format video image sensor**
- **Selectable EIA(NTSC) or CCIR(PAL) Output**
- **Selectable mirror image**
- **Auto gain control (maximum + 18 dB)**
- **High I.R. sensitivity for nighttime applications**
- **Auto and manual backlight compensation mode**
- **Gamma correction -On/Off**
- **External frame sync capability**
- **40mw on chip power consumption**
- **External data acquisition support**
- **Smear free**
- **Auto Level expanding**
- **Optional Edge enhancement**

General Description

The OV5116 is a complete black and white CMOS Video Camera chip. It conforms to EIA (60 Hz) and CCIR (50 Hz) standards and outputs composite video capable of directly driving a 75Ω display device. The OV5116 also offers built-in video output switching, allowing several OV5116 chips to share the same display without the need for external video multiplexing units.

The on-chip auto exposure allows for a wide range of lighting conditions, eliminating the need for external mechanical shutter components. This, along with its single supply, low power consumption makes the OV5116 an incredibly versatile and cost-effective video camera perfect for the following types of applications:

- Security
- Surveillance
- Machine Vision
- Process control
- CCTV
- Infant monitoring
- Toys



OV5116 PIN ASSIGNMENT

Array Size	**EIA(NTSC):** 320 x 240 pixels **CCIR(PAL):** 352 x 288 pixels
Effective Image Area	3.2 x 2.5mm
Auto Electronic Exposure (seconds)	1/50-1/6000
Minimum Illumination	0.5 lux @ f 1.4 (3000k)
S/N Ratio	46 dB (AGC=1x)
Power Supply	5VDC, ±5%
Power Requirements	(40 mw before-loading), 70mw standard loading
Package Type	28 pin LCC

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1. Introduction

This section describes the features and functions of the OV5116, a monochrome CMOS video camera integrated circuit.

2. Pin Assignments:

Table 1. Pin Descriptions

Pin #	Name	Class	Function
1, 2, 20, 23, 26	AVDD, SVDD, DVDD, OVDD DEVDD	Bias	Power (+5V) connections.
3	VRCHG	OA	Internal voltage reference. Connect to AGND with a 0.1uF capacitor.
4	N50	I-Ø	EIA mode with 50hz light
5	ABOFF	I-Ø	Auto level descending function off
6	VCBRT	OA	Output Black level, leave it open in usual case
7, 21, 25, 28	SGND, DGND, DEGND, AGND	Bias	Ground connections. Connect to supply common.
8	EIA	I-1	Mode select input. Logic high(1)=EIA mode; low(Ø)=CCIR mode.
*9	BKLT	I-Ø	Backlight mode 1
10	XTAL2	XO	Oscillator clock output or crystal output.
11	XTAL1	XI	External oscillator input or crystal input. Use 12.288MHz for EIA mode, 13.5MHz for CCIR mode.
12	FSI	I-Ø	External frame sync input. A rising edge on FSI sets the chip timing to vertical sync. Leave open if unused.
13	OENB	I-Ø	A logic level input to enable or tri-state CVO. Logic high(1)=tri-state;low(Ø)=enabled.
14	G4X	I-Ø	A logic level input which when high places the maximum AGC gain to 4x. When low the sensor AGC gain is 2x.
15	FAST	I-Ø	A logic level input to enable/disable AGC/AEC FAST mode. High enables, low disables, which provides slow and smooth AGC/AEC mode.
16	BPED	I-Ø	A logic level input to disable on chip edge enhancement. High disable, low enable.
17	GAMMA	I-1	A logic level pin to select the transfer characteristic of output voltage versus light input. Logic high for g=0.45; low for g=1.
18	FSO/MIRR	I/O Ø/Ø	In/out pin.Frame Sync Output. Digital frame sync output pin. Positive pulse occurs during the CVO vertical sync period. Input is a logic level input to enable mirror function
19	PCLK/G8X	I/O Ø/Ø	Digital pixel clock output. Provides 2 functions: When high a valid pixel is present at CVO and in sync with PCLK. Input is a logic level input to enable maximum AGC gain to 8x (only effective when pin 14 is set to high(1))
22	CVO	Q	The composite video output signal. The output is a source follower capable of directly driving a 1V p-p signal into a 108 ohm load.
*24	ATBLK	I-Ø	Backlight mode 2
27	VREQ	OA	Internal voltage reference level. Connect to AGND with a 0.1uF capacitor.

*** Pin 9 and Pin 24 must be used in a logical combination as per the following table:**

ATBLK(Pin 24)	BLKT(Pin 9)	Mode
Ø	Ø	Normal Mode
Ø	1	Mode 1 - Manual Back light
1	Ø	Mode 2 – Automatic Back light (Chip determination)
1	1	Future Use

Class	Default Level
I-1	digital input, with 100k pull up
I-Ø	digital input, with 100k pull down
I/O	digital CMOS level input and output
OA	analog CMOS reference voltage
O	75W output
XI/XO	crystal input/output
Bias	power supply bias

Ø: Low; O: Output

3. Electrical Characteristics

Table 2. Electrical Parameters

PARAMETER	CONDITIONS	MIN	TYP	MAX	Units
VDD	Power supply voltage	4.75	5.00	5.25	volts
Vpeak	CVO output peak voltage*		1.0		volts
Vblnk	CVO output blank voltage*		0.4		volts
Vsync	CVO output sync voltage*		0		volts
IDD1	Functioning with 108Ω load on CVO			15	mA
IDD2	Functioning with 10k load on CVO			6	mA
Cin	Maximum pin capacitor			10	pF
f_{osc}	crystal/ceramic resonator frequency: EIA - 60Hz CCIR - 50Hz		12.288 13.5		MHz MHz
t_{cyc}	pixel clock cycle time: EIA - 60Hz CCIR - 50Hz		163 148		ns ns
t_r, t_f	Maximum digital input rise/fall time			20	ns

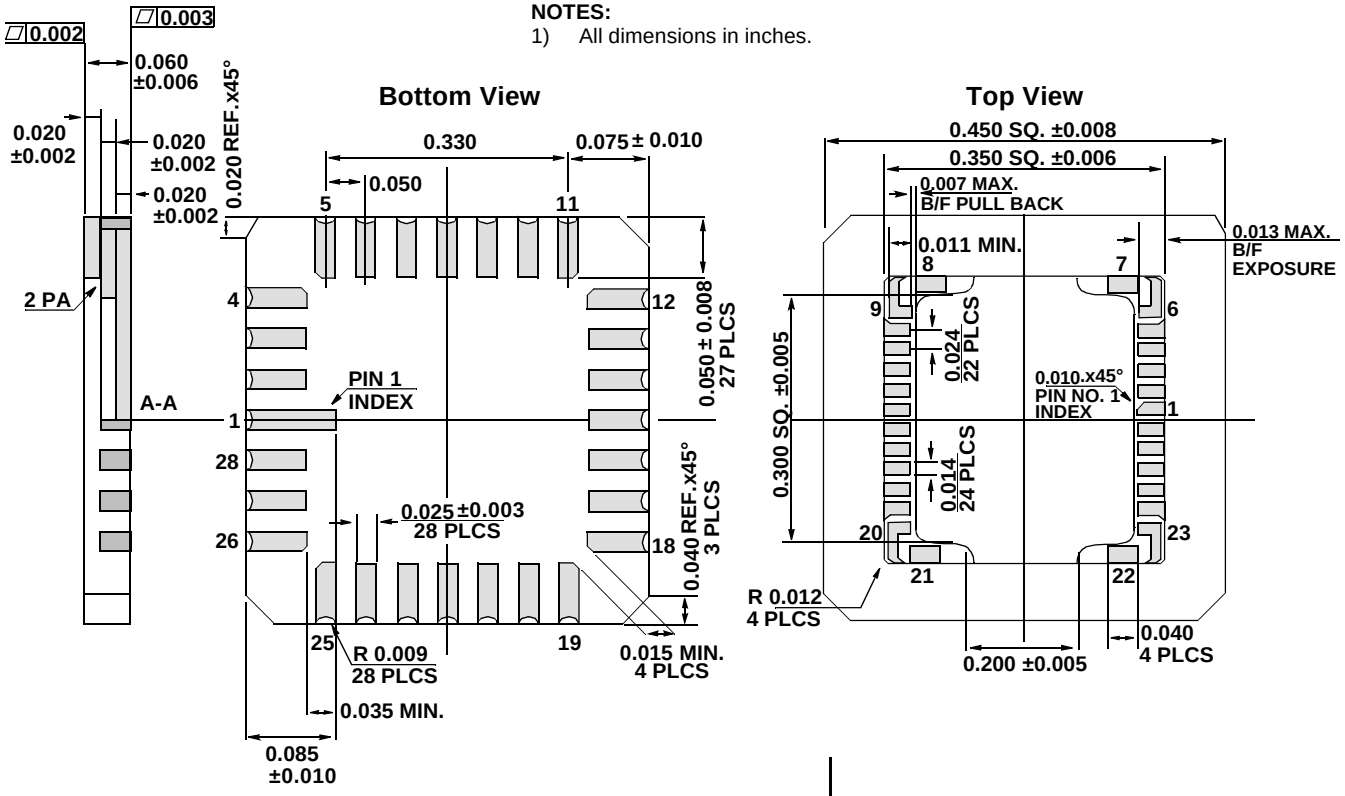
* assuming standard loading of 108Ω (33Ω+75Ω).

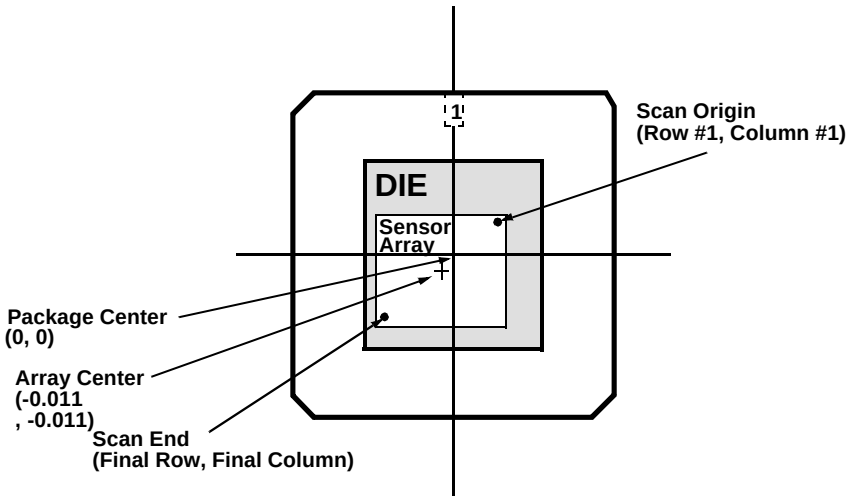
Table 3. OV5116 TV Timing Specification

	Parameters	CCIR	EIA	Unit
1	number of lines per frame	625	525	lines
2	field frequency	50.00	60.01	Hz
3	line period	64.0	63.476	µsec
4	line blanking interval	11.84	11.41	µsec
5	line synchronizing pulse	4.73	4.56	µsec
6	field blanking interval	24/25	22/23	line
7	first equalizing pulse width	3/2.5	3/2.5	line
8	field synchronizing pulse width	2.5	3	line
9	second equalizing pulse width	2.5/3	2.5/3	line
10	FSO width	2.5	3	line

Figure 1. OV5116 Series Package and Sensor Array Dimensions

NOTES:
1) All dimensions in inches.





Top View

Note: Most lens assemblies reverse the viewed scene onto the sensor array, which generally means that pin 1 should be located at the bottom of the p.c. board. To ensure correct display orientation, check the lens specification prior to laying out the printed circuit board.

OV5016 Module Reference Design (Do not use for new design)

The following reference design module changes need to be done to the below OV5016 module reference design when performing a change over from the OV5016 IC to the OV5116 IC:

R4 68 change to 33 ohms

R6 remove = Gamma on; leave on = Gamma off

R1 remove auto back light (effect is minimal)

R3 remove

R2 remove back light (effect is minimal)

R8 remove

Note: The above changes to the OV5016 reference design module for supporting the OV5116 IC will result in an improved image.

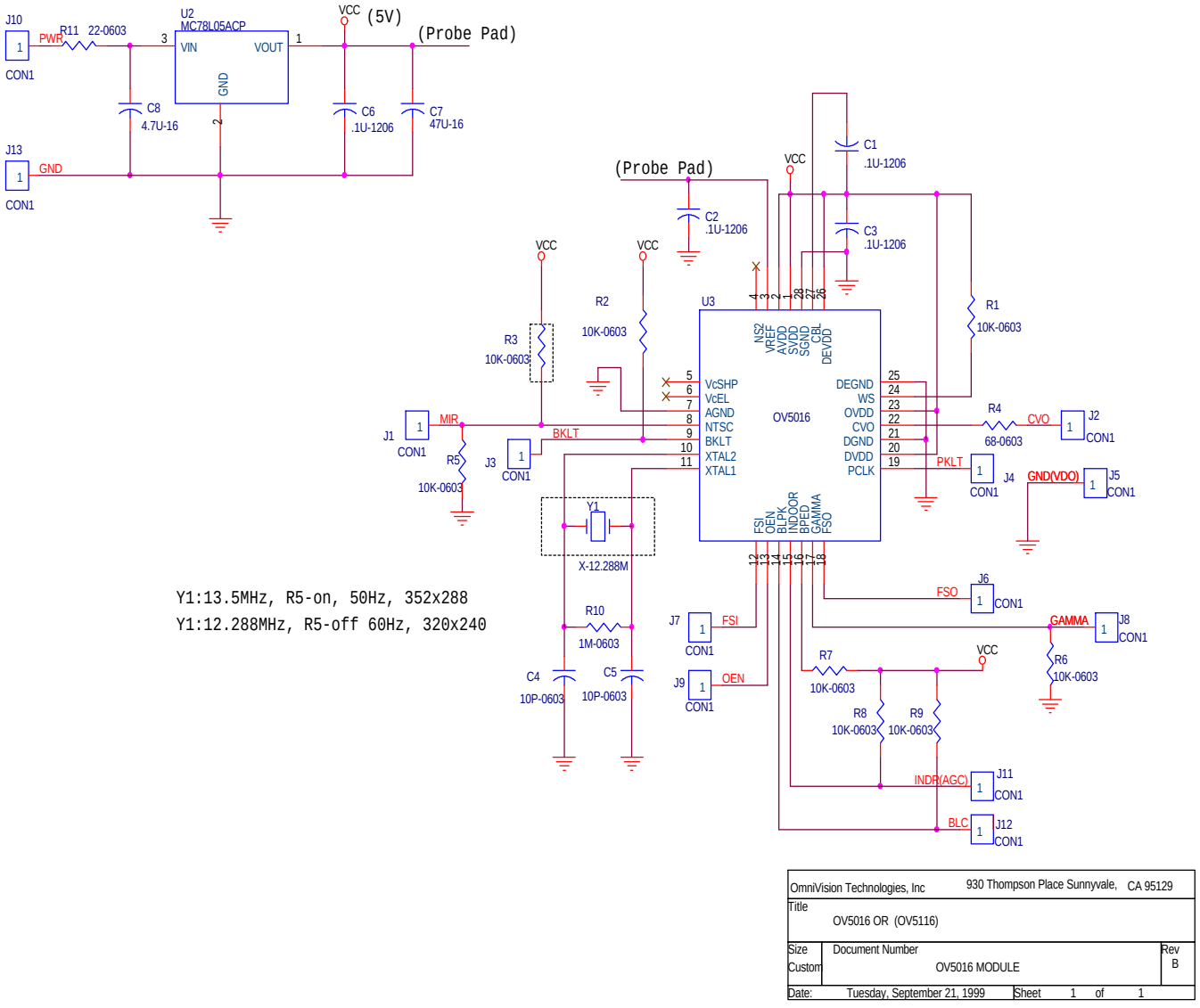


Figure 2. *OV5016 Module Reference Design (Do not use for new design)*

OV5116 Module Reference Design (Use for all new designs)

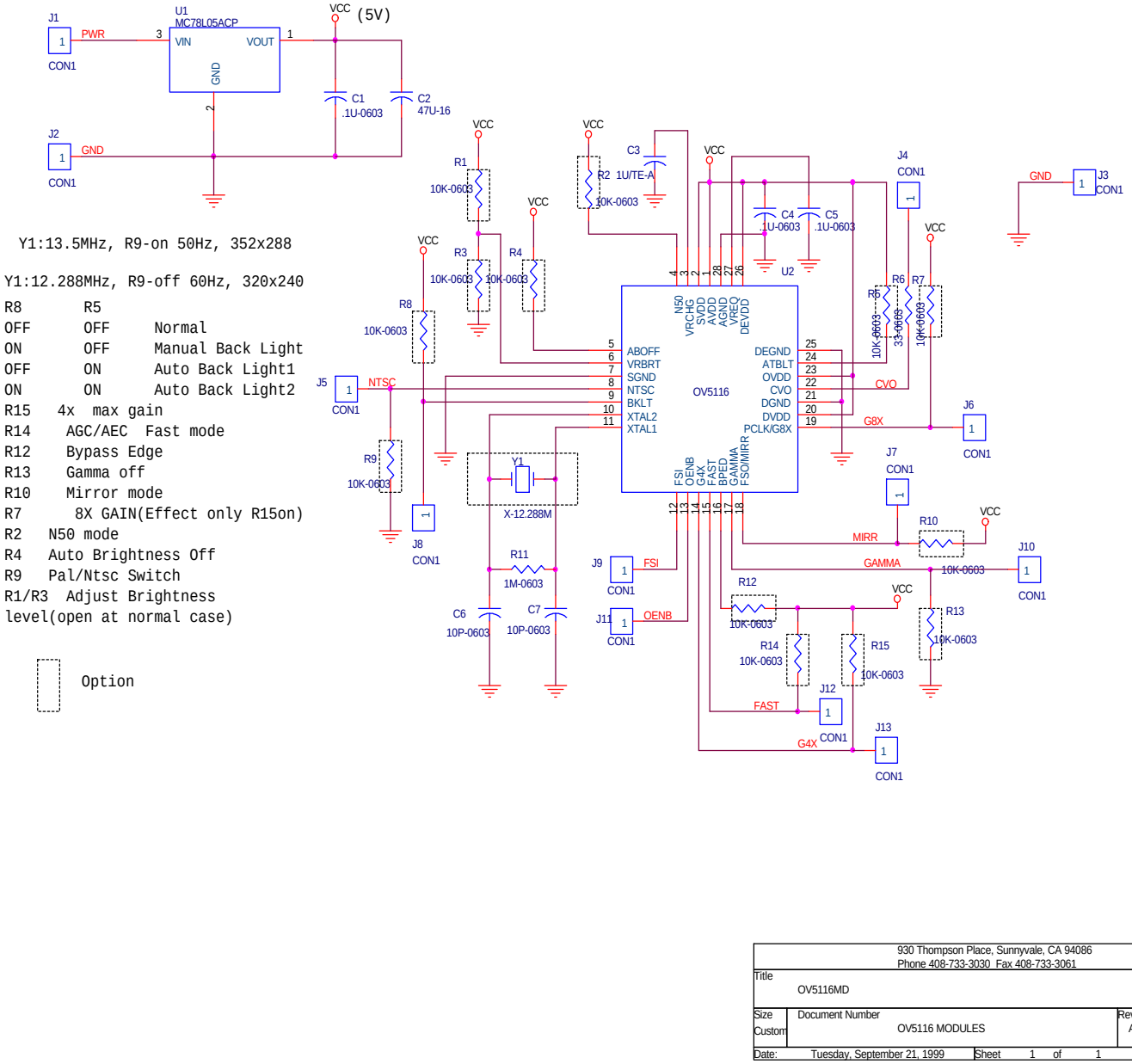


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Figure 3. Reference Design for OV5116 (Use for all new designs)