



KEELOQ Code Hopping Decoder Using Secure Learn

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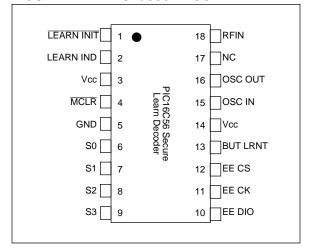
OVERVIEW

This application note fully describes the working of a code hopping decoder implemented on a Microchip PIC16C56 microcontroller. This decoder uses the secure learn (seed-based) method of learning new transmitters. This application note describes the various KEELOQ® code hopping encoders that can be used with the decoder, the decoder hardware, and the various software modules comprising the system. The software can be used to implement a stand alone decoder or integrate with full function security systems. The decoder supports the Microchip HCS200, HCS300, HCS301, HCS360, HCS361 and HCS410 KEELOQ Code Hopping Encoders.

KEY FEATURES

- · Stand alone decoder
- Compatible with Microchip HCS200, HCS300, HCS301, HCS360 HCS361 and HCS410 encoders
- · Automatic bit rate detection
- · Automatic encoder type detection
- · Four function outputs
- · Six learnable transmitters
- · RC Oscillator

FIGURE 1: PIC16C56 DECODER



Notice:

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Microchip's Secure Data Products are covered by some or all of the following patents:
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INTRODUCTION TO KEELOQ ENCODERS

All KEELOQ encoders use the KEELOQ code hopping technology to make each transmission by an encoder unique. The encoder transmissions have two parts. The first part changes each time the encoder is activated and is called the hopping code part and is encrypted. The second part is the unencrypted part of the transmission, principally containing the encoder's serial number identifying it to a decoder. Refer to DS91002, *Introduction to KEELOQ*.

Hopping Code

The hopping code contains function information, a discrimination value, and a synchronization counter. This information is encrypted by an encryption algorithm before being transmitted. A 64-bit encryption key is used by the encryption algorithm. If one bit in the data that is encrypted changes, the result is that an average of half the bits in the output will change. As a result, the hopping code changes dramatically for each transmission and can not be predicted.

Function Information

The encoder transmits up to four bits of function information. Up to 15 different functions are available.

Discrimination Value

Stored in the encoder EEPROM, this information can be used to check integrity of decryption operation by a decoder. If known information is inserted into the transmitted string before encryption, the same information can be used at the decoder to check whether the information has been decrypted correctly. In the Microchip HCS encoders, up to 12 bits (including overflow bits) are available.

Synchronization Counters

The transmitted word contains a 16-bit synchronization counter. The synchronization information is used at the decoder to determine whether a transmission is valid or is a repetition of a previous transmission. Previous codes are rejected to safeguard against code grabbers.

The HCS300, HCS301 and HCS410 encoders transmit two overflow bits which may be used to extend the range of the synchronization counter from 65,536 to 196,608 button operations. The HCS360 and HCS361 encoders transmit one overflow bit which can be used to extend the range of the synchronization counter from 65,536 to 131,071 button operations.

Unencrypted Code

Serial Number

The encoder's serial number is transmitted every time the button is pressed. The serial number is transmitted unencrypted as part of the transmission and serves to identify the encoder to the decoder.

Other Status and Function Information

The HCS200, HCS300, and HCS301 encoders include provision for four bits of function information and two status bits in the fixed code portion of its transmission. The two status bits indicate whether a repeated transmission is being sent, and whether the battery voltage is low. The HCS200 does not send repeated transmission information, and the bit is permanently set to '0'.

The HCS360/361 encoders transmit two bits that are used as a Cyclic Redundancy check. These bits can be used to check the integrity of the reception. Additionally, the HCS360 and HCS361 encoders can extend the length of the serial number from 28 bits to 32 bits, replacing the unencrypted function code.

Seed Transmissions

The Microchip HCSXXX encoders all have the ability to transmit a fixed seed. The seed value is programmed into the encoder when the encoder is first initialized along with the counters, key, serial number, and other information. The seed length differs from encoder to encoder with the HCS200, HCS300, and HCS301 having a 32-bit seed. The HCS360 and HCS361 encoders have a 48-bit seed. The HCS410 has a 60-bit seed. Table 1 summarizes seed transmissions in the Microchip HCSXXX encoders.

TABLE 1: KEELOQ ENCODER SEED TRANSMISSION SUMMARY

| Encoder | Seed Length | Seed Transmission Activation |
|---------|-------------|---|
| HCS200 | 32 bits | Seed transmitted immediately if S0, S1, and S2 are activated. |
| HCS300 | 32 bits | Seed transmitted immediately if S0, S1, S2, and S3 are activated. |
| HCS301 | 32 bits | Seed transmitted immediately if S0, S1, S2, and S3 are activated. |
| HCS360 | 48 bits | Seed transmitted immediately if S0 and S3 are activated. Seed transmitted after 3 seconds if S0 and S1 are activated. |
| HCS361 | 48 bits | Seed transmitted immediately if S0 and S3 are activated. Seed transmitted after 3 seconds if S0 and S1 are activated. |
| HCS410 | 60 bits | Seed transmitted immediately if S0, S1 and S2 are activated. Seed transmitted after 3 seconds if S0 and S1 are activated. |

Transmission Format Summary

Table 2 contains a summary of the information contained in transmissions from each of the KEELOQ encoders that can be learned by the Microchip decoder.

FIGURE 2: DECODER BLOCK DIAGRAM

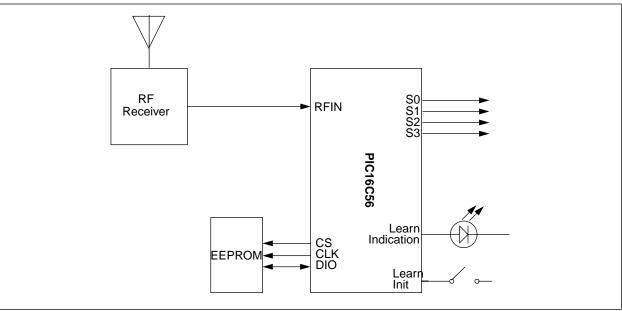


TABLE 2: KEELOQ ENCODER TRANSMISSION SUMMARY

| | HCS200/201 # of bits | HCS300/301 # of bits | HCS360/361 # of bits | HCS410 # of bits |
|---------------------------|-------------------------|-------------------------|-------------------------|---------------------|
| Total Transmission Length | 66 | 66 | 67 | 69 |
| Code Hopping Portion | 32 | 32 | 32 | 32 |
| Sync Counter | 16 | 16 | 16 | 16 |
| Discrimination bits | 12 | 10 | 8 | 10 |
| User Bits | 0 | 0 | 2 | 0 |
| Overflow Bits | 0 | 2 | 1 | 2 |
| Independent Mode | 0 | 0 | 1 | 0 |
| Function Code | 4 | 4 | 4 | 4 |
| Fixed Portion | 34 | 34 | 35 | 37 |
| Serial number | 28 | 28 | 28/32 | 28/32 |
| Function Code | 4 | 4 | 4/0 | 4/0 |
| Low Voltage Indicator | 1 | 1 | 1 | 1 |
| Repeat Bit | 1 | 1 | 0 | 0 |
| CRC | 0 | 0 | 2 | 2 |
| Queue Bits | 0 | 0 | 0 | 2 |

TABLE 3: HCS200/201 AND HCS300/301 CODE HOPPING TRANSMISSION FORMAT

| Code Hopping Portion | | | Fixed Portion | | |
|----------------------|----------------|------|---------------|------|--------------|
| Sync Counter | Discrimination | Func | Serial Number | Fund | VLOW REPT |

TABLE 4: HCS200/201 AND HCS300/301 SEED TRANSMISSION FORMAT

| Seed Portion | Fixed Portion | | |
|--------------|---------------|------|------|
| Seed | Serial Number | Func | VLOW |
| | | | REPT |

TABLE 5: HCS360/361 CODE HOPPING TRANSMISSION FORMAT

| Code Hopping Portion | | | Fixed Portion | | |
|----------------------|----------------------------|------|-------------------------------|--------------|--------------|
| Sync Counter | Discrimination OVR, IND | Func | Serial Number (28/32 bits) | Func (4/0 | VLOW REPT |
| | | | , | bits) | |

TABLE 6: HCS360/361 SEED TRANSMISSION FORMAT

| Seed Portion | Fixed Port | ion | |
|-------------------|----------------------------------|--------------|--------------|
| Seed (48 bits) | Serial Number (12/16 MS bits) | Func (4/0 | VLOW REPT |
| | , | bits) | |

TABLE 7: HCS410 CODE HOPPING TRANSMISSION FORMAT

| Code Hopping Portion | | | Fixed Portion | | |
|----------------------|-----------------------|------|-------------------------------|-----------------------|--------------------|
| Sync Counter | Discrimination OVR | Func | Serial Number (28/32 bits) | Func (4/0 bits) | VLOW CRC QUE |

TABLE 8: HCS410 SEED TRANSMISSION FORMAT

| Seed Portion | Fixed Portion | |
|--------------|---------------|------|
| Seed | Func | VLOW |
| (60 bits) | (4/0 | CRC |
| | bits) | QUE |

PWM Format

In general, all KEELOQ encoders share a common transmission format:

A **preamble** to improve biasing of decision thresholds in super-regenerative receivers. The preamble consists of alternate on and off periods, each lasting as long as a single elemental period.

A **calibration** header consisting of a low period of 10 elemental periods. Calibration actions should be performed on the low period of the header to ensure correct operation with header chopping.

A **string** of pulse-width modulated bits, each consisting of three elements. The first element is high, the second contains the data transmitted and is either high or low, the third element is always low.

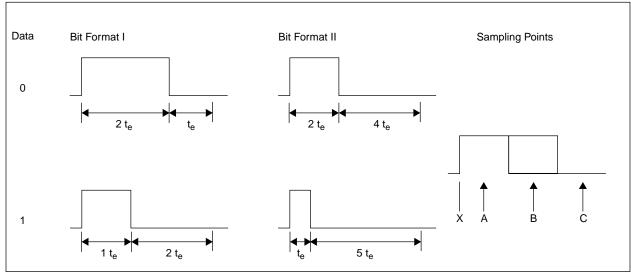
A **guard** period is usually left between the transmissions. During this period nothing is transmitted by the encoder.

Figure 3 shows the sampling points when sampling the data bits. The first and last elements are used exclusively to verify the integrity of the received symbol. The first element (sample point A) is always high, the second (sample point B) is the complement of the data bit being sent, and the final element (sample point C) is always low. Because the period between the low portion of a bit (sample point C) and the rising edge of the following bit (sample point X) can vary, the rising edge of the first element (sample point X) is used to resynchronize the receiving routine to each incoming bit.

If random noise is being received, the probability of a set of three samples producing a valid combination is only $2^{-2} = 1/4$. For a string of 66 bits, the corresponding figure is 2^{-134} .

Integrity checking on incoming signals is important. Code hopping signals require significant processing, as well as EEPROM access, to decrypt. Unnecessary processing can be avoided by not attempting to decrypt incoming codes that have bit errors.

FIGURE 3: KEELOQ PWM TRANSMISSION FORMAT



DECODER IMPLEMENTATION

The Microchip decoder's primary hardware components are a PIC16C56 RISC microcontroller and a 93LC46B EEPROM as shown in the decoder schematic in Figure 10. However, this solution can be implemented in any PICmicro® microcontroller with at least 1K words of program memory. The operating frequency of the controller is 4 MHz. The microcontroller is used to capture transmissions from the various encoders, decrypt transmissions captured, and check the validity of the transmission based on the information in the decrypted transmission and information stored in the EEPROM. If a transmission from a valid encoder is received, the decoder activates the outputs dictated by the transmission.

Encoder information, such as serial number, synchronization information, and decryption key is stored externally in an EEPROM. The EEPROM used is a Microchip 93LC46B Microwire[®] Serial EEPROM. The information stored in the EEPROM is encrypted to protect the contents. The EEPROM encryption is less secure than the KEELOQ code hopping algorithm.

As can be seen from the section on encoder transmissions, there are differences in the transmission formats of the different encoders that can be used with the decoder. The following section summarizes how the differences in transmitted data are dealt with by the decoder.

As the serial number information follows after the code hopping portion of the transmission, any number of serial number bits can be received and processed. In the Microchip decoder described, the complete serial number (28 bits) is stored.

The serial number is used to identify the memory block used to store the 64-bit decryption key for a particular encoder because of the relationship between serial number, seed, and the decryption key. In other words, the serial number is stored with the key. When a transmission is received, the decoder finds the correct memory block by checking all blocks until a matching serial

number is found. The key is then retrieved from that particular memory block. A serial number of 0000000₁₆ is considered invalid and is ignored by the decoder.

After matching the received and stored serial number, validation of a received transmission consists of two steps. The first includes checking the integrity of the decryption operation. Here the decoder compares the 12-bit discrimination value received with the stored discrimination value. The discrimination value stored with the HCS300/301/360/361/410 includes overflow bits and user bits.

The second portion of validation involves checking synchronization information for that particular encoder. The synchronization counter transmitted by all encoders is 16 bits long. Two copies of the full synchronization counter are stored for all valid encoders. The storing of two copies of the synchronization information protects the decoder from loosing synchronization with an encoder if one of the counters is corrupted.

PINOUTS OF MICROCHIP KEELOQ DECODER

FIGURE 4: FUNCTIONAL INPUTS AND OUTPUTS

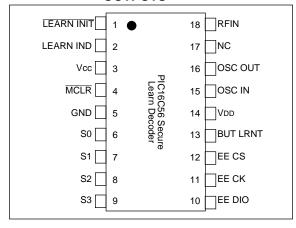


TABLE 9: MICROCHIP DECODER FUNCTIONAL INPUTS AND OUTPUTS

| Mnemonic | Pin Number | Input / Output | Function |
|----------------|------------|----------------|--|
| RF IN | 18 | I | Demodulated PWM signal from RF receiver. The decoder uses this input to receive encoder transmissions. |
| LEARN INIT | 1 | I | Input to initiate learning, active low. |
| LEARN IND | 2 | 0 | Output to show the status of the learn process (in an integrated system this will be combined with the system status indicator). |
| BUT LRNT | 13 | 0 | Indication that the received function code matches the learned function code. |
| S0, S1, S2, S3 | 6, 7, 8, 9 | 0 | Function outputs—corresponds to encoder input pins. |

PROGRAM FLOW

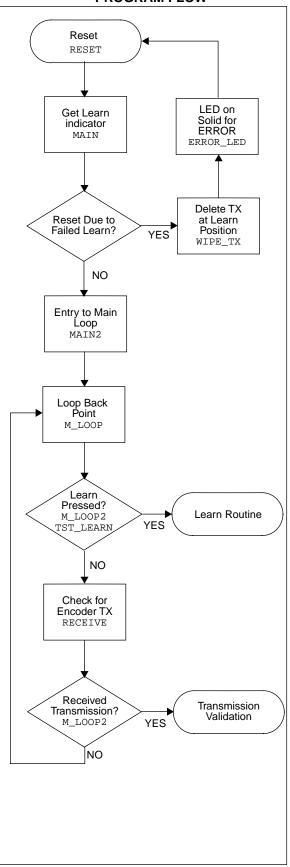
The software for the Microchip decoder has been written for the PIC16C56 microcontroller. The compiler used is MPASM version 01.30.01. The operating frequency of the PIC16C56 is 4 MHz. The clock speed should be kept as close as possible to 4 MHz as the reception routine (RECEIVE) is dependent on the 4 MHz clock for correct functioning. Other decoder functions that rely on a 4 MHz clock speed are the hold times of the various outputs and time-outs. The main program flow is described here. Detailed descriptions of individual functions can be found further in the application note.

As can be seen from Figure 5, the decoder reads the learn indicator, which stores the next position to be overwritten when the decoder enters a learn sequence and decoder status flags, from the external EEPROM on power-up. The status flags are checked to see if a learn routine was interrupted when the microcontroller was reset. If so, it is assumed the learn cycle was not successfully completed, and the encoder at the learn indicator is subsequently deleted (WIPE_TX).

The encoder then enters the main loop where it spends most of its time. The main loop checks to see if the learn button is being activated (TST_LEARN). If so, the decoder enters the learn mode described in the "Learn" section in AN652.

If learn has not been initiated, the microcontroller then checks for transmissions from encoders (RECEIVE). If a transmission from an encoder has successfully been received, the microcontroller validates the transmission received as described in the "Transmission Validation" in AN652. If the transmission received is a valid transmission from an encoder learned into the system, the system sets the appropriate outputs (M_BUT).

FIGURE 5: MICROCHIP DECODER MAIN PROGRAM FLOW



FUNCTIONAL MODULES

Reception

The reception routine (RECEIVE) is based on a reliable algorithm which has successfully been used in previous implementations of KEELOQ decoders. Automatic bit-rate detection is used to compensate for variations in bit rate of different encoders of a specific type, as well as the differences in bit rate between different encoders (HCS200, HCS300, and HCS360). The reception routine is able to receive 64-bit transmissions. This is easily extended to receive more bits. The reception routine is able to determine the number of bits in the transmission.

The reception algorithm performs a number of functions when an output is detected from the receiver. Figure 6 gives all the major sampling points in the reception algorithm.

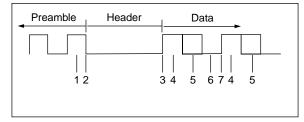
The reception algorithm calibrates on the low period of the header to determine the actual elemental period for the transmission being received. The required elemental period is 10% of the low header period. In Figure 6 the header calibration sample points are marked 1 through 3. The calibration flow chart (Figure 7) shows at what points in the program samples 1, 2, and 3 are taken.

Elemental periods outside the capture range of the algorithm (either too long or too short) are rejected, since they are due either to noise or to reception of an incomplete signal.

Using the determined elemental period, three samples after the first rising edge (Sample 3) following the header are taken. The first sample is taken half an elemental period after the rising edge (Sample 4); the second, one elemental period later (Sample 5), and the third, another one elemental period later (Sample 6). The first sample must be high, the second could be either high or low, and the third sample must be low. If either the first or the third sample is not as expected, the attempt at capturing a transmission is abandoned. In Figure 6, the data sample points are points 4 through 6. The flow chart describing data reception (Figure 8) shows where in the code the samples are taken.

If all 66 bits have been captured, each with the correct first and third elements, the transmission can be assumed to be correct, and decryption can commence. The receiving routine should be called often enough to ensure that the high portion in the header is not missed (Sample 1, Figure 6).

FIGURE 6: SAMPLING POINTS USED IN RECEIVE ALGORITHM



In systems where the reception routine is called to check if there is activity on the receiver input, the routine should poll the input for a valid transmission for at least the time taken to complete one transmission if activity is detected on the input line. This makes provision for the reception routine being called while a transmission is in progress. Having missed the first header, the first transmission will be invalid and be discarded. The decoder should continue sampling the input through the guard time in order to catch the next header and transmission (i.e., for a decoder designed to capture HCS300 transmissions the time spent polling for a valid transmission should be at least 100 ms if activity is detected in the input line).

Reception Algorithm Flow Chart

The first flow chart (Figure 7) describes the calibration routine which is used to determine the actual transmission rate of the encoder so that the decoder can compensate for deviations from nominal timing. There are four different exit points, each of which should branch to a point in the program where housekeeping and input monitoring can be resumed. There is only one exit point for a valid calibration operation (RCV7). At this point, it is assumed that a valid header has been received and that a string of data bits will follow.

The second flow chart (Figure 8) handles the reception of bits once the calibration routine has been successfully completed. The data bits are all sampled three times each to ensure that a noise free transmission has been received. The reception routine uses the calibrated elemental period, determined in the calibration routine, to ensure that the samples are correctly spaced. The routine resynchronizes itself on the rising flank of each bit. Only 60 bits of the data received are used by the Microchip decoder described, the decoder ignores the unencrypted function code and the status bits.

If the control samples in a given bit are sampled correctly (i.e., the first element is high and the last element is low), the routine checks whether more than 56 bits have been received correctly. If not, the routine returns to the calling procedure.

FIGURE 7: **CALIBRATION FLOW CHART**

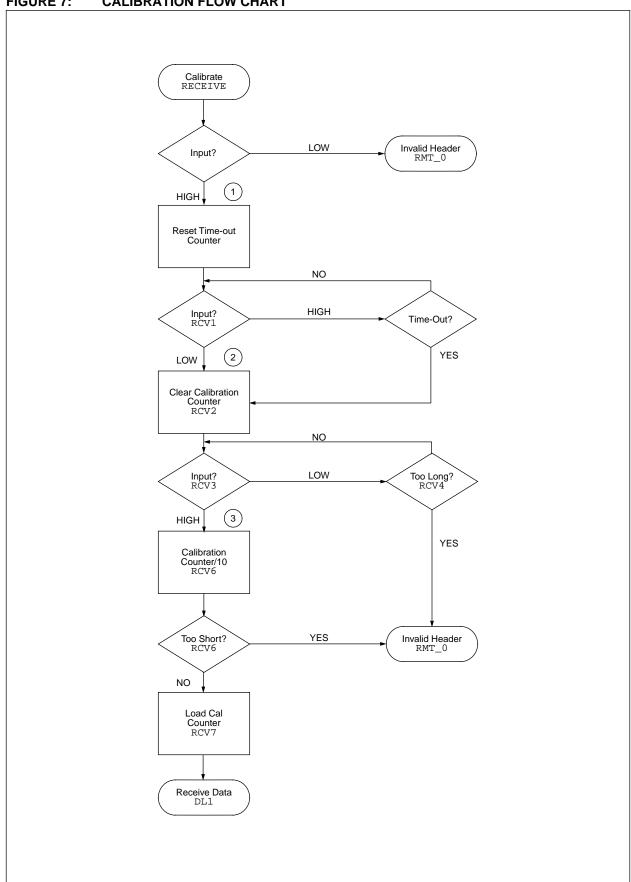


FIGURE 8: **DATA RECEPTION FLOW CHART** Receive Data RCV7 (3) Wait Half Bit Period DL1 LOW Input SAMPLE1 (4) HIGH Wait Full Bit Period DL2 (5) HIGH Input SAMPLE2 LOW Data = 0 Data = 1 Set Up DL1 Timer RCV11 Wait Full Bit Period DL3 HIGH (7)Input RCV8/RCV9/ RVC10 HIGH Input SAMPLE3 LOW (6) LOW NO NO Time-out? Last Bit? YES YES Received NO Invalid 56 Bits? RMT01 YES Reception Complete Cleanup RMT2 RMT1

VALIDATION
SYNCHRONIZATION
FUNCTION INTERPRETATION
OUTPUT ACTIVATION
KEY GENERATION
DECRYPTION
LEARN
ROM MEMORY MAP
EEPROM MEMORY MAP
RAM MEMORY MAP

The confidential and proprietary information contained in this section of AN652 has been removed. The full application note is available under a license agreement and can be ordered as DS40149 from Microchip Technology Inc.

DEVICE PINOUTS

The device used in the application note is a PIC16C56 PDIP.

TABLE 10: DEVICE PINOUTS

| PIN | PIC16C56 Function | Decoder Function | PIN | PIC16C56 Function | Decoder Function |
|-----|-------------------|------------------|-----|-------------------|--------------------------|
| 1 | Port A Bit 2 | LEARN Input | 18 | Port A Bit 1 | RF Input |
| 2 | Port A Bit 3 | LRN INDICATOR | 17 | Port A Bit 0 | Not used |
| 3 | TIMER0 | Connect to VDD | 16 | Osc In | RC osc (4 MHz) |
| 4 | MCLR | Brown out detect | 15 | Osc Out | |
| 5 | GND | Ground | 14 | VDD | +5V supply |
| 6 | Port B Bit 0 | S0 | 13 | Port B Bit 7 | BUT LRNT |
| 7 | Port B Bit 1 | S1 | 12 | Port B Bit 6 | CS (93LC46B, pin 1) |
| 8 | Port B Bit 2 | S2 | 11 | Port B Bit 5 | CLK (93LC46B, pin 2) |
| 9 | Port B Bit 3 | S3 | 10 | Port B Bit 4 | DIO (93LC46B, pin 3 & 4) |

TIMING PARAMETERS

TABLE 11: TIMING PARAMETERS

| Parameter | Typical | Unit |
|--|---------|------|
| Output activation duration | 524 | ms |
| Output pause if new function code received | 131 | ms |
| Erase all duration | 8.4 | s |
| Learn mode time-out | 33.6 | s |
| Learn successful LED flash duration | 4.2 | s |
| Learn successful LED flash rate | 3.8 | Hz |
| Learn failure LED on duration | 1 | S |

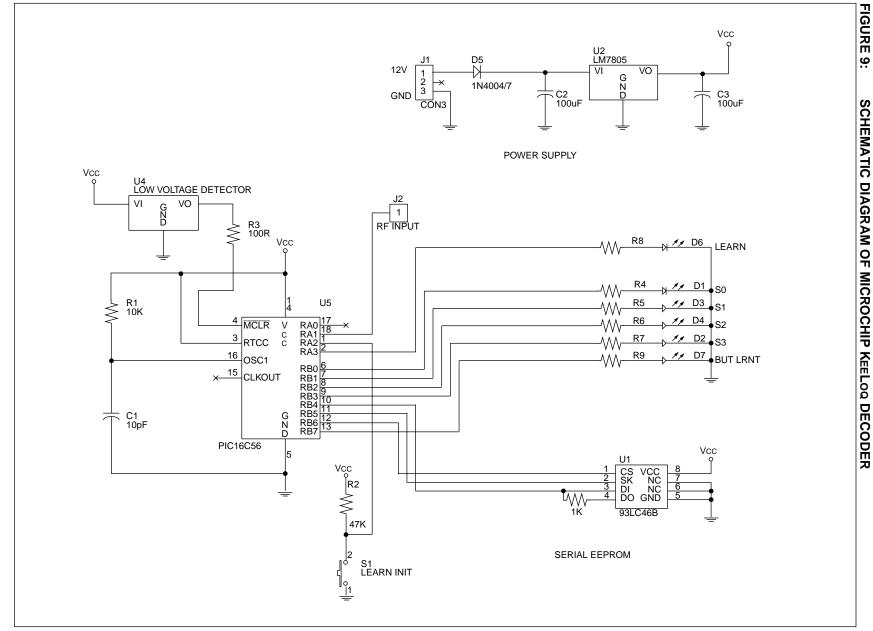
SOURCE CODE LISTING

A diskette is supplied containing source code for the Microchip decoder in the file MSLRN**.ASM. The code has been compiled using MPASM v01.30.01. Certain functions are dependent on the oscillator speed for correct functioning. Examples of time dependent functions include RECEIVE and TST_RTCC. The PIC16C56 Microcontroller should run at 4 MHz.

TABLE 12: LIST OF IMPORTANT FUNCTIONS

| Function Name | Description | | |
|---------------|--|--|--|
| CALC_KEY | Key generation routine. | | |
| DECRYPT | Decryption routine for Hop Code. | | |
| EEREAD | The data in the EEPROM at ADDRESS is read and decrypted to TMP1 and TMP2 (Note). | | |
| EEWRITE | The data in TMP1, and TMP2 is encrypted and written to the EEPROM at ADDRESS (Note). | | |
| M_DIS | Check discrimination value. | | |
| M_CNT | Check synchronization (counter) values. | | |
| RECEIVE | Start of the RF reception routine. | | |
| TST_LEARN1 | Check for learn mode and entry to learn. | | |
| TST_RTCC | Check TIMER0 and do whatever real time tasks are required. | | |

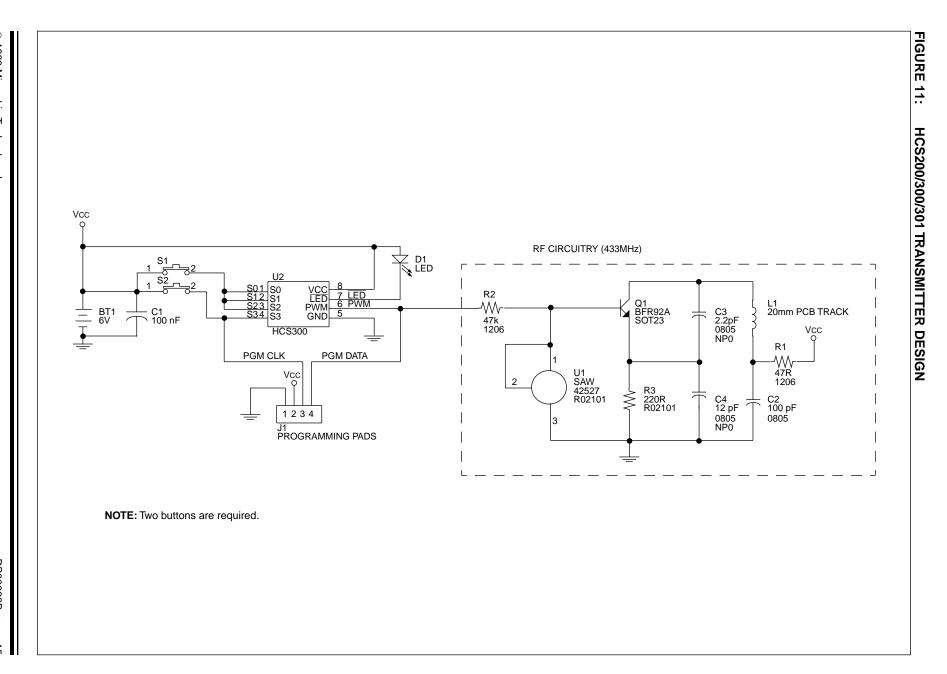
Note: TMP1, TMP2 and ADDRESS are user defined registers.



D10

S1 LEARN INIT

LEARN



NOTES:



NOTES:

NOTES:

Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet.
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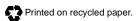
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